

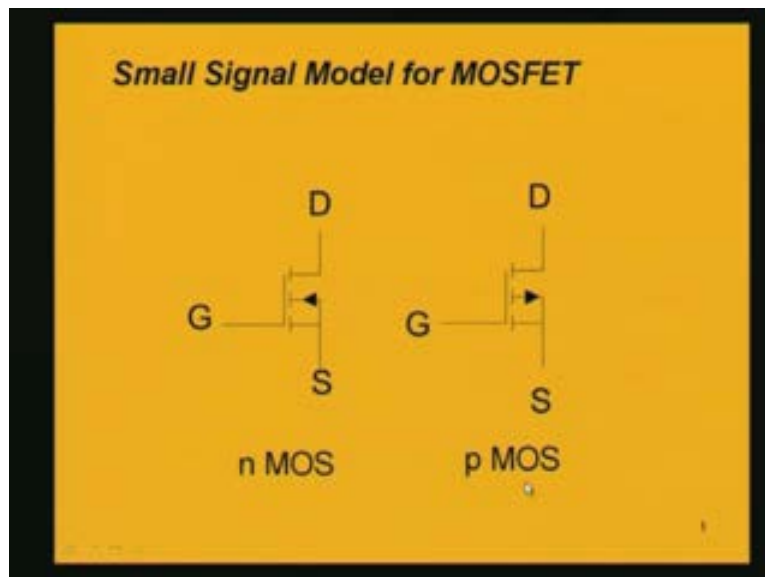
Basic Electronics
Prof. Dr. Chitrlekha Mahanta
Department of Electronics and Communication Engineering
Indian Institute of Technology, Guwahati

Module: 3 Field Effect Transistors
Lecture-5
Small signal model of MOSFET – Part I

We have been discussing about the MOSFET used as an amplifier. In the earlier classes we have seen how the MOSFET device can be used for amplification of a weak signal and we also saw the different biasing circuits which are used in the amplifier. Today we will discuss about the MOSFET amplifier by using the small signal model for the MOSFET device. Earlier in the discussion about the BJT as an amplifier we have followed the similar procedure. We found out the small signal equivalent circuit for the device and replacing this device by its small signal equivalent circuit we proceeded to find out the parameters related in the amplifier like input impedance, output impedance, voltage gain, etc. Similarly today we will discuss how the small signal equivalent circuit for the MOSFET device is developed and using this small signal equivalent circuit in the amplifier network we will proceed to find out the different parameters which are related to the amplifier.

First let us discuss how the small signal equivalent circuit can be drawn? We take the n-channel and p-channel enhancement type MOSFET. We are continuing our discussion with enhancement type MOSFET. Symbolic representation of this enhancement type MOSFET is as shown here where we are taking the n MOS and p MOS.

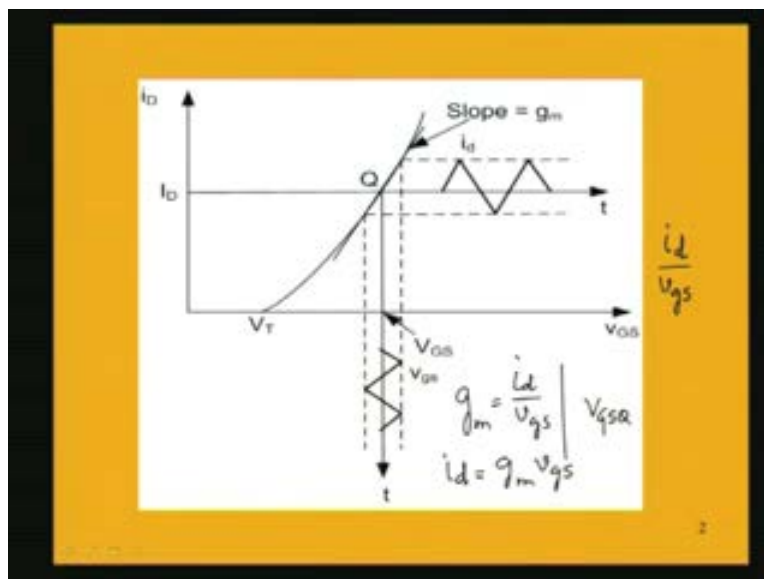
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n MOS meaning the n-channel MOSFET and p MOS is a p-channel MOSFET and both we take are the enhancement type MOSFET device. We have three terminals drain, gate and source. How to develop the small signal equivalent circuit? Always we find out the behavior of the device from its characteristics and from the characteristic we represent the device to show equivalently the characteristic with representation by some parameters which will be best fitted for that device. For example in this enhancement type MOSFET device, if we look into the characteristics one characteristic we found earlier that was the transfer characteristic which was between the drain current and the gate to source voltage. Similarly another characteristic curve which we studied earlier was the VI characteristic or the drain characteristic that shows the behavior of the drain to source current with respect to the drain to source voltage for various values of the gate to source voltage. Let us recollect those two characteristics because these characteristics are the key for finding out the small signal model.

In the transfer characteristic that we discussed earlier that is nothing but a nonlinear characteristic curve drawn between the drain current and the gate to source voltage and if only the DC condition is taken then the operating point signifies the condition for DC and when we apply a small signal between gate and source then the slope for this characteristic will give you a parameter which is the transconductance that we already know. The transconductance we have found out from the i_d by v_{gs} . That was for small signal i_d by v_{gs} . Around this operating point we took the slope for this curve. We are taking both i_d by v_{gs} are small signal at the operating point that is represented by V_{GSQ} . Around the operating point a small region is taken to find out the slope and this slope i_d by v_{gs} that gives you the transconductance; that we earlier found out. This transconductance will be used for drawing the small signal equivalent model. This is an important parameter as far as the device is concerned because if you notice from this representation the drain current is $g_m v_{gs}$.

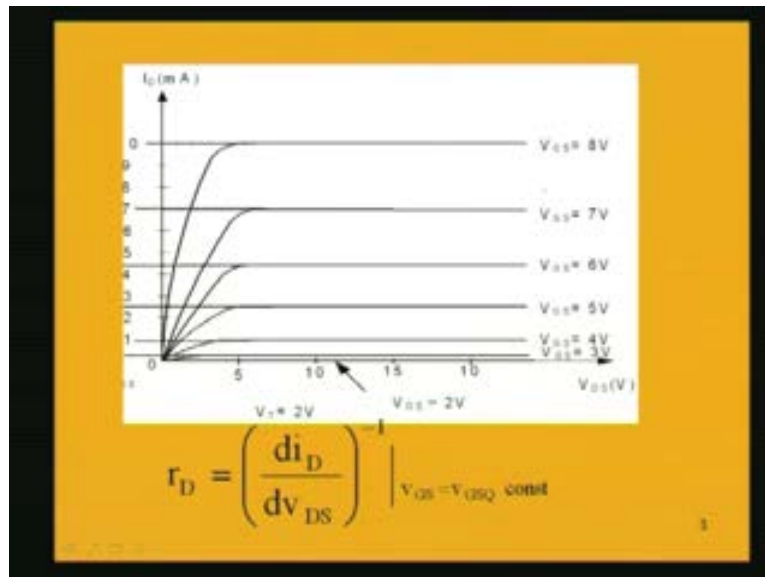
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It is like a current source. The drain to source is a current source which is represented by transconductance for the device multiplied by this small gate to source voltage. As we are dealing with the small signal we are discussing an amplifier. This is an important parameter the transconductance which we found out from the transfer characteristics by finding out the slope around the operating point.

Another characteristic which will be used for finding out the small signal model is the drain characteristic, the characteristic or the relation of the drain current versus the drain to source voltage for various values of the gate to source voltage. We get a family of curves and if we consider at a particular gate to source voltage that is the operating point because we are operating the amplifier with a biasing circuit which will set the operating point or the quiescent point that particular value of this V_{GS} is known.

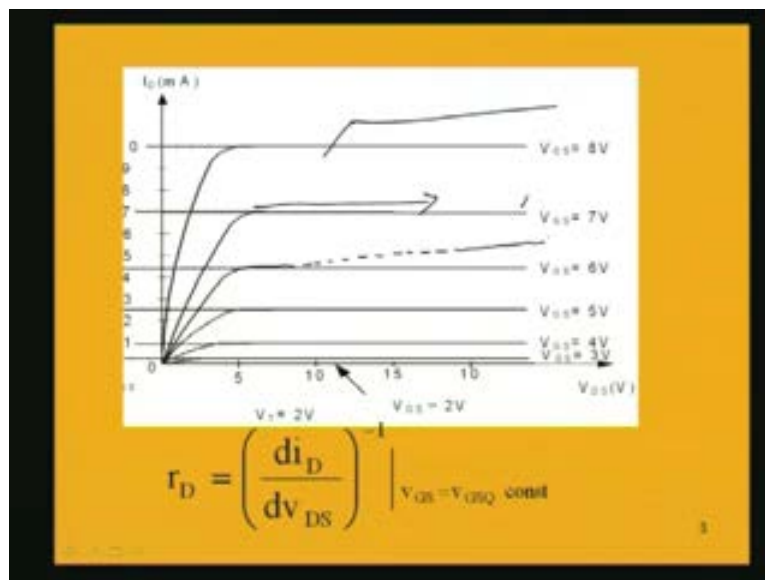
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For that particular V_{GS} if we consider the whole characteristic we will now focus only on a single curve which will be for that particular gate to source voltage. Suppose this is the gate to source voltage or that is the operating point gate to source voltage. Then we will be interested in this curve. As far as this characteristic is concerned one important parameter which will be taken from this curve is the output resistance. Here we see that the saturation region is the region where the amplifier will be used. You will use the MOSFET amplifier under saturation. This is the saturation region and you will be interested in this region only. For practical consideration we can see that this resistance at the output, the drain to source resistance whichever is existing between drain to source that resistance is quite high. It is almost infinite; from the curve itself it is very clear. As it is horizontal, even if you go on increasing the drain to source voltage the drain current does not vary in the saturation region and that signifies that the output resistance between drain to source is very, very high, infinite in fact.

But practically speaking or in fact what happens is that there is a little slope to the right in the output characteristics for a particular curve. That happens because if we go on increasing the drain to source voltage then the channel length decreases. We have earlier discussed at the pinching off that when drain to source voltage is increased then the saturation will occur because there will be very, very small number of charge carriers present in the channel and finally it will reach saturation and beyond saturation even if you increase this drain to source voltage the current does not increase. But in fact there is a rise of current when the drain to source voltage is increased beyond saturation to high value because the channel length reduces and actually what happens is that because of the high drain to source voltage, the charge carriers will be just swept away from the channel and it will accumulate in the drain. So there is a rise in the current because the length is reduced means current is inversely proportional to the channel length. Basically what happens is it will increase. Current increases when you go on increasing the drain to source voltage and that is why there is actually a rise in slope to the right. Although the curve is horizontal as it is shown but practically there is a little slope to the right.

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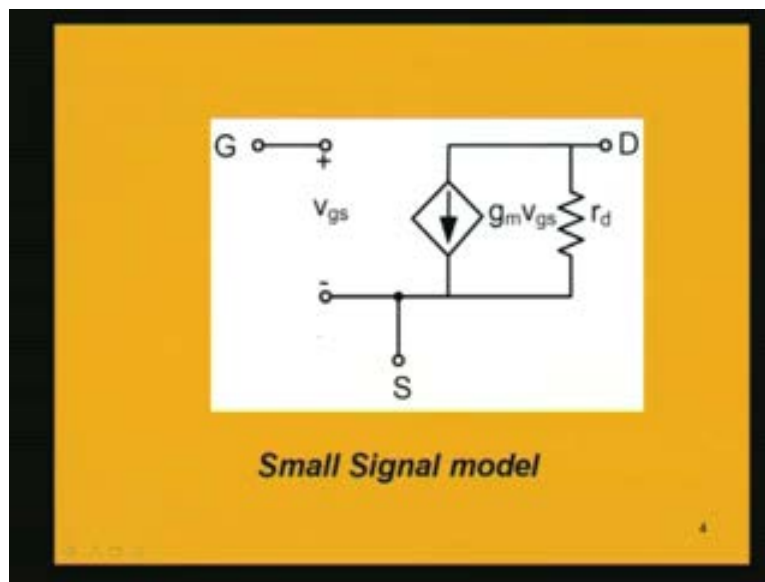


As there is a little slope in the IV characteristic curve that means that we have a finite output resistance between the drain and the source. It is in fact not infinite it is having a finite value. Although it may be very high in the order of mega ohm range say but still it will be finite. That resistance let us name by r_D . D subscript is used for drain resistance. Drain to source part will have a resistance which is di_D by dv_{DS} inverse. That means it is the derivative between the drain current and the drain to source voltage, inverse with V_{GS} constant at the operating point that is for a particular V_{GS} . Suppose this V_{GS} we are considering for that gate to source voltage for the operating point at which we are using the amplifier with the biasing scheme, then at that operating point if we find out the resistance between drain and source it is given by this expression. As it is clear it is the inverse of the slope between the current and the voltage because the slope between

current and the voltage will be the admittance, inverse of the resistance but we will replace the part between the drain and source by its resistance. But sometimes you will find mostly that the specification in the data sheet gives admittance y_o . If y_o is given that is the admittance between the drain and source, its inverse will give you the resistance between drain and source at that operating point. With the knowledge of these two, one is the transconductance and the other is the drain to source resistance we can very easily draw the small signal equivalent model for the e MOSFET, enhancement type MOSFET that is being considered now.

Let us draw that. Here this is the small signal equivalent model having three terminals gate, drain and source. The gate terminal and the source terminal as we can see here are having in between voltage v_{gs} that is the gate to source voltage and the open circuit between gate and source signifies that gate current is zero. Because we know from our earlier consideration or studies that gate current is zero because input resistance is very, very high almost infinite.

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There is no flow of gate current. Gate current is zero means the input resistance between gate and source is high. That is why it is represented by the open circuit between the gate and source and if we consider the other side between drain and source, as we have just now discussed, the current source between drain and source that is the drain current which is represented by $g_m v_{gs}$, it is the current source between drain and source and apart from that there will be the output resistance between the drain and source which is represented by small r small d . That can be found out from the specification of the data sheet. If we are given the admittance we can take the reciprocal and find out the resistance. This is the small signal equivalent circuit or small signal model for this MOSFET. Both n-channel and p-channel enhancement type MOSFET will have the small signal representation.

In this circuit the important parameters which are to be noted are g_m and r_d . These are the inherent parameters of the device. v_{gs} is the small signal between gate to source. Basically that is the input voltage which is the ac voltage you will apply, which needs to be amplified. We are having a model which can be used for replacing the actual physical MOSFET device and using this small signal and fitting it into the amplifier network we will find out the different parameters. We will use this small signal model. This small signal model is for the device, so that has to be kept in mind.

In BJT also we have a transistor. That transistor is equivalently modeled electrically by this small signal model. Depending upon what circuit you are going to use for the amplifier, the whole network will have its AC equivalent circuit and in that AC equivalent circuit the device part is replaced by this model. We are going to basically see what different configurations are there for the MOSFET amplifier? Before going into that let us now note one point that the transconductance which we have found out from the transfer characteristic that we derived earlier has a value of $2 K_n V_{GS}$ minus V_T . We have found that by using the transfer characteristic here by finding out the ratio between small i_d and v_{gs} . There is another way to find out this transconductance. The definition of transconductance is actually $\frac{di_D}{dv_{GS}}$.

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For Enhancement - type MOSFETs,

$$g_m = \frac{i_d}{v_{gs}} = 2k_n (V_{GS} - V_T)$$

g_m can also be found out by taking

$$\left. \frac{di_D}{dv_{GS}} \right|_{V_{GS}=V_{GSQ} \text{ const}} \quad g_m = \frac{\Delta i_D}{\Delta v_{GS}}$$

in $i_D = k_n (v_{GS} - V_T)^2$

Here we are considering instantaneous values. Small i capital D, small v capital GS means it is instantaneous values because the small change or ratio between the incremental changes can be found out by finding out the derivative provided the derivation of this derivative is at the operating point. That is why v_{GSQ} ; at that point constant v_{GSQ} means at the operating point gate to source voltage we are finding out this derivative. We know the current expression. There you have to find out the derivative with respect to GS. We have this expression i_D ; mind it this is the instantaneous value of current that is given by K_n , the device constant which is the fabrication constant into v_{GS}

minus V_T whole square. V_T is the threshold voltage. In this expression we will find out the derivative of i_D with respect to v_{GS} . If I do that then this derivative with respect to V_{GS} will give me twice K_n into V_{GS} minus V_T . Both the ways we finally get the same value. That is the same expression we get by finding the transconductance in both the ways. One way is from the transfer characteristic and here we are finding out by the derivative. This expression can be further written in another way because we know that $V_{GS} - V_T$ equal to from this expression if we write it will be under root i_D by K_n . We can write it as $2K_n$ under root i_D by K_n but this is at the V_{GSQ} , operating point. So we have to replace this value of V_{GS} . That is why for this small v_{GS} I am writing capital V_{GS} , so at that value of voltage the current is nothing but DC current. That is the operating point current value. That is we will write Q at operating point. It can be written as root K_n into capital I capital DQ .

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The image shows a handwritten derivation of the MOSFET transconductance g_m on a yellow background. The equations are as follows:

$$i_D = k_n (v_{GS} - V_T)^2$$

$$\therefore g_m = \left. \frac{di_D}{dv_{GS}} \right|_{V_{GSQ}} = 2k_n (V_{GSQ} - V_T)$$

$$= 2\sqrt{k_n I_{DQ}}$$

$$2k_n \sqrt{\frac{I_{DQ}}{k_n}} \Delta \theta$$

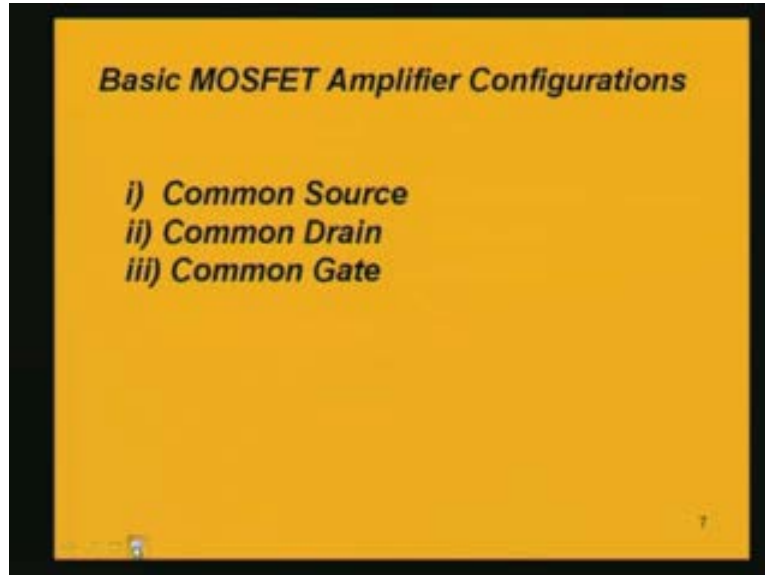
$$= 2\sqrt{k_n I_{DQ}}$$

On the right side, there is a separate equation: $V_{GS} - V_T = \sqrt{\frac{i_D}{k_n}}$. A curved arrow points from this equation to the $(V_{GSQ} - V_T)$ term in the main derivation.

This is another expression to represent the transconductance. Once you know K_n , once you know the operating point DC drain current, i_d then we can find out the trans conductance. We have seen that the MOSFET device is having its small signal model representation. There are different types of configurations of the MOSFET amplifier where we will use this small signal model.

There are three types of configuration for the MOSFET amplifier. One is the common source MOSFET amplifier, second is the common drain configuration of MOSFET amplifier and the third one is the common gate.

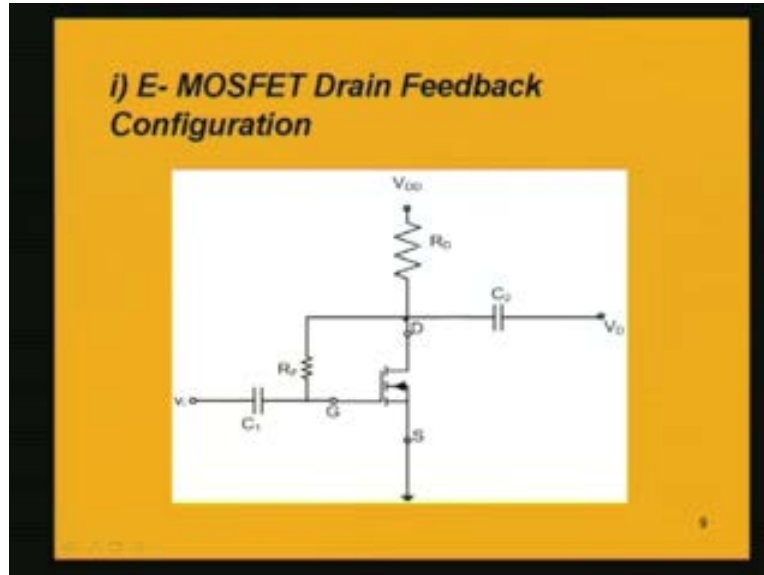
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In BJT also we have got three configurations for amplifier. One is common emitter, then common collector and then common base. Similarly corresponding configurations for MOSFET amplifier will be common source, common drain and common gate. We will first discuss about the common source MOSFET amplifier, the configuration of common source. As the name suggests common source means that source will be common to both input and output circuits and it will be grounded. Now let us discuss about the common source MOSFET amplifier and then find out the different parameters related to common source MOSFET amplifier using the biasing schemes that we discussed earlier. We earlier discussed the feedback biasing scheme and voltage divider biasing scheme. Using these two biasing schemes we will build the MOSFET amplifier and we will find out the parameters like input impedance, output impedance, voltage gain, etc.

Let us first take the drain feedback configuration. In the feedback biasing scheme the drain is having a feedback resistance to the gate and it is an enhancement type MOSFET that we are discussing and to have the conformity with our earlier discussion we are taking n-channel enhancement type MOSFET. The drain feedback means we have a resistance between this drain and this gate. That value R_f is the resistance. It is common source. As far as the source is concerned you can say that the source is grounded and we have an input voltage v_i that is ac signal which is applied at the input. There is a biasing voltage V_{DD} which will be required. For the biasing scheme we know that this DC voltage is required for the biasing part and that is there V_{DD} through a resistance R_D .

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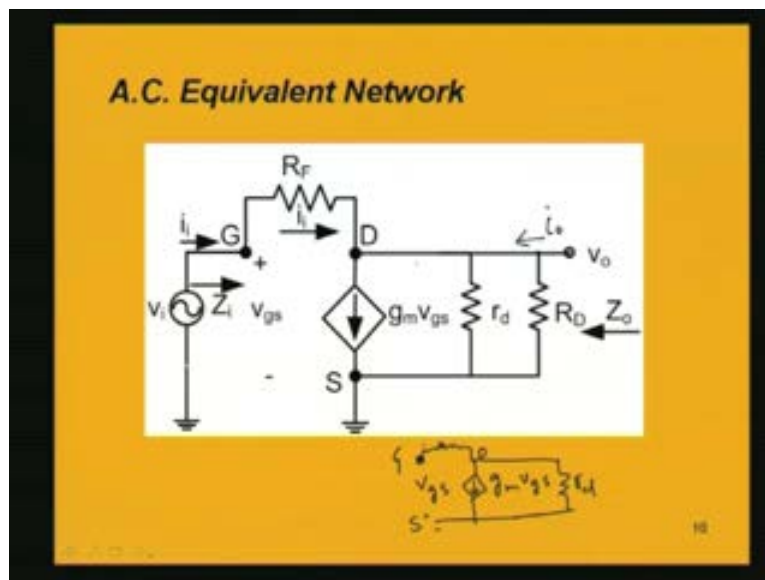
This is the drain terminal, gate terminal and source terminal and we have the voltage at this end of the drain. There are coupling capacitors and the need for this coupling capacitor is well understood by now because earlier also we had this coupling capacitors in the BJT amplifiers. The purpose of using the coupling capacitors are to separate the DC and AC. We want to block the DC and at the output here we must get purely AC voltage. That is why the coupling capacitor is there, C_2 is there. Similarly this C_1 is present to isolate the DC components from the source that is the signal v_i . This is a simple feedback biasing scheme. Here what will be doing that the part which is coming from the MOSFET device, as you can see here this is the MOSFET device and we will represent this MOSFET device by its small signal model. The small signal model which we just arrived at will be used to represent this MOSFET device. The other part we will further draw the equivalent AC because earlier also we have seen that when you analyze the AC circuit we are concerned about the AC conditions. As the characteristics whatever we are using these are basically assumed to be linear. The DC condition and AC conditions are separated out. They can be combined as far as linear analysis is concerned. That way we will first draw the AC equivalent for this network. You know that the drawing of AC equivalent requires that the DC biases be grounded, made zero and the capacitances generally have high values so that we can practically assume the capacitances to be short circuited under AC. As far these two capacitances are concerned at that frequency of operation where we are using that amplifier the capacitances will be practically short circuited. Short circuiting means straight connection of a short circuiting wire; there is no resistance. Doing that whatever part can be bypassed by this short circuit part, will be bypassed and finally we will draw the equivalent network. Let us do that here. This V_{DD} will be made zero. These two capacitances will be short circuited, rest remaining same and this device will be represented by its small signal model.

We arrive upon this AC equivalent network. This is the small signal equivalent model. As we have seen the gate and source are open circuited in the small signal model of the

device and we have the transconductance and this resistance. Small signal model was having G , S ; v_{gs} was this voltage between these two and we had this drain to source current $g_m v_{gs}$ and this was the r_d . This was the small signal model and in between gate and drain here we see that there is this resistance R_f . The drain and gate terminals will have the resistance as seen here. R_f resistance is the feedback resistance between drain and gate and also the drain is now having a resistance R_D connected to ground because if we look here, V_{DD} will be short circuited. If it is drain terminal we will have a resistance to ground.

From drain to ground we have a resistance R_D because V_{DD} is made zero. That is what is done here; from drain we have a resistance R_D to ground and this is the input voltage V_i which is applied at the gate terminal; here we are applying the V_i . This capacitance is short circuited so it is directly having this V_i . In this network we now find out the parameters like input impedance, output impedance, voltage gain, etc. We know that input impedance is equal to input voltage by input current. So V_i by i_i is Z_i . When we look from the input terminals into the network, the resistance or impedance Z_i is V_i by i_i and output impedance is v_o by i_o . i_o is actually this; towards the device it is flowing.

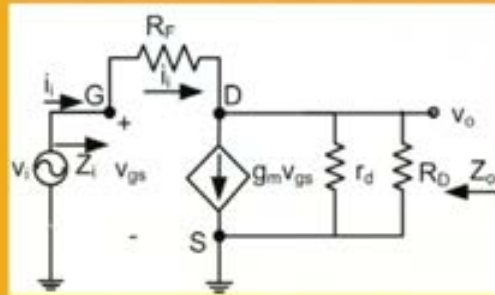
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Let us find out what is Z_i ?

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To find parameters Z_i , Z_o , A_v



The parameters which will be of our concern are Z_i , Z_o , A_v . We will find out input impedance, output impedance and voltage gain. As per definition we will proceed. Let us first find out what is the input impedance Z_i ?

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Z_i Input Impedance

Applying KCL at node D

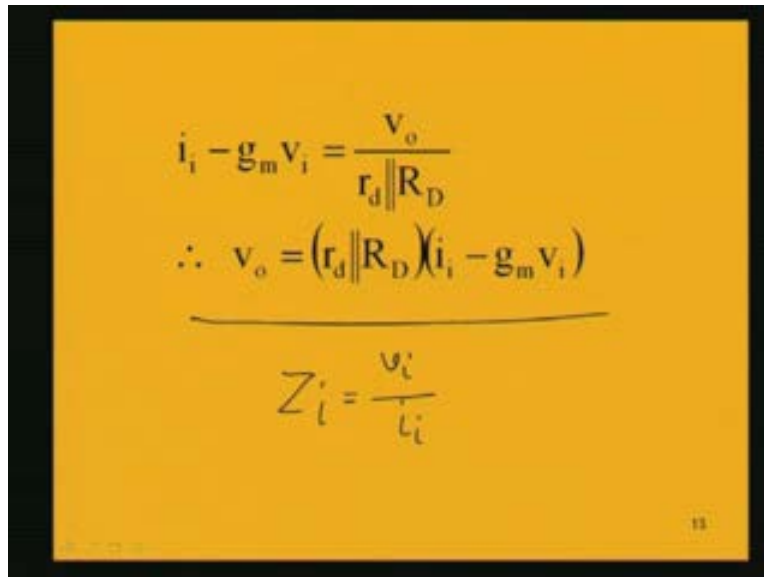
$$\begin{aligned} i_i &= g_m v_{gs} + \frac{v_o}{r_d \parallel R_D} \\ &= g_m v_i + \frac{v_o}{r_d \parallel R_D} \end{aligned}$$

To find out input impedance we will have to now look into the input circuit. That is here if you give your attention to the drain terminal and apply the Kirchoff's current law at the drain terminal, sum of the incoming current is equal to the sum of outgoing currents. Here at the drain incoming current is the input current i_i . We see here i_i , the input current is flowing through the resistance R_F also because there is no gate current or there is no other current at this terminal. This current is flowing through R_F . This is incoming to the

drain. So i_i is equal to sum of the outgoing currents. We look into the drain terminal and find out that the outgoing currents. One is this current from drain to source given by $g_m v_{gs}$. The other current which flows through this part can be found out by finding out the equivalent impedance between these two resistances and dividing V_o by this equivalent resistance because the current which flows in this part is again having two parts. One is through this small r_d one is through this capital R_D . The current can be found out; voltage here is v_o divided by equivalent of this two resistances small r_d parallel capital R_D . This is the current say i_i equal to this one. Now we can write down the Kirchoff's current law at the drain terminal which is i_i equal to $g_m v_{gs}$ plus v_o by small r_d parallel capital R_D .

But this gate to source voltage, v_{gs} is input voltage v_i . So replacing this v_{gs} by v_i we get this expression. We write it in another way. i_i minus $g_m v_i$ equal to v_o by r_d parallel capital R_D . What is v_o ? Let us express v_o from this equation. If you cross multiply v_o is equal to r_d parallel R_D into i_i minus $g_m v_i$. This expression we get for output voltage. We will utilize this expression to find out the input impedance. Because input impedance is input voltage by input current.

(Refer Slide Time: 37:59)



$$i_i - g_m v_i = \frac{v_o}{r_d \parallel R_D}$$

$$\therefore v_o = (r_d \parallel R_D)(i_i - g_m v_i)$$

$$Z_i = \frac{v_i}{i_i}$$

We need to find out this expression by rearranging. Here we are only getting an expression for v_o but we have to find out what is v_i by i_i . For that again we look into the circuit and what is this current i_i ? It can be written as the potential difference between this gate and drain divided by this resistance. That is the potential difference or the voltage drop between these two points the gate and the drain is v_i minus v_o . Here this voltage is v_i and here the voltage is v_o . v_i minus v_o by R_F equal to i_i . Let us write that v_i minus v_o by R_F equal to i_i , input current. Now what we will do is we will find out i_i by replacing v_o which we have already found.

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$$\begin{aligned}
 \text{Again, } i_i &= \frac{v_i - v_o}{R_F} \\
 \text{or, } i_i &= \frac{v_i - (r_d \parallel R_D)(i_i - g_m v_i)}{R_F} \\
 i_i R_F &= v_i - (r_d \parallel R_D)i_i + (r_d \parallel R_D)g_m v_i \\
 v_i [1 + g_m (r_d \parallel R_D)] &= i_i [R_F + r_d \parallel R_D]
 \end{aligned}$$

That way it is equal to v_i minus v_o we represent from here; v_o equal to r_d parallel capital R_D into i_i minus $g_m v_i$ divided by R_F . Cross multiplying we get i_i into R_F equal to v_i minus multiplication of this two term, if I break it open it will be minus r_d parallel R_D i_i minus, minus plus r_d parallel capital R_D into $g_m v_i$. We take the terms having v_i . We collect the terms, combine them so that will be v_i into this is the one term having v_i , this is another term having v_i and the others terms have i_i . Our job is simple because we need to find the ratio between v_i and i_i . There are two terms having v_i and i_i ; we collect them. v_i into 1 plus $g_m r_d$ parallel R_D that is equal to i_i into R_F plus r_d parallel capital R_D . From this expression we need to find out the ratio between v_i and i_i which is the input impedance. Input impedance Z_i equal to v_i by i_i , which is equal to this R_F plus r_d parallel capital R_D by 1 plus $g_m r_d$ parallel capital R_D . This expression is the exact expression for the input impedance.

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$$Z_i = \frac{v_i}{i_i} = \frac{R_F + r_d \parallel R_D}{1 + g_m r_d \parallel R_D}$$

Approximation

$$Z_i \cong \frac{R_F}{1 + g_m r_d \parallel R_D}$$

if $R_F \gg r_d \parallel R_D$

We can approximate this expression to find an easier representation if certain conditions are met. Here we can see that in this whole term in the numerator and denominator there are R_F , r_d and capacitor R_D , three resistances. The values of the resistances are such that generally the feedback resistance is quite high in comparison with the other component which is small r_d parallel capacitor R_D . If we look into this parallel combination of the small r_d and capacitor R_D basically what happens is when you take that parallel combination between two unequal resistances, one very high and the other very small, the parallel equivalent will tend to or approach the smaller value. Here r_d is quite high in comparison to R_D . What will be the final equivalent parallel combination? It will approach capacitor R_D and compared to this parallel combination equivalent we have the feedback resistance sufficiently higher. So in the numerator this whole term can be approximated. This term r_d parallel capacitor R_D is almost equal to R_F . Doing that basically we get a simpler version that is why we are doing this exercise. In the numerator it will be R_F in the denominator I am keeping as it is.

Again further approximation can be done utilizing the fact that the resistances small r_d and capacitor R_D are such that practically the small r_d is quite high. This the thumb rule actually. The thumb rule says that if small r_d is greater than or equal to 10 times the capacitor R_D then we can further simplify this expression by writing down in the denominator only capacitor R_D . Instead of small r_d parallel capacitor R_D , it will boil down to capacitor R_D only. Small r_d parallel capacitor R_D will boil down to capacitor R_D only if this condition is met.

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Further Approximation

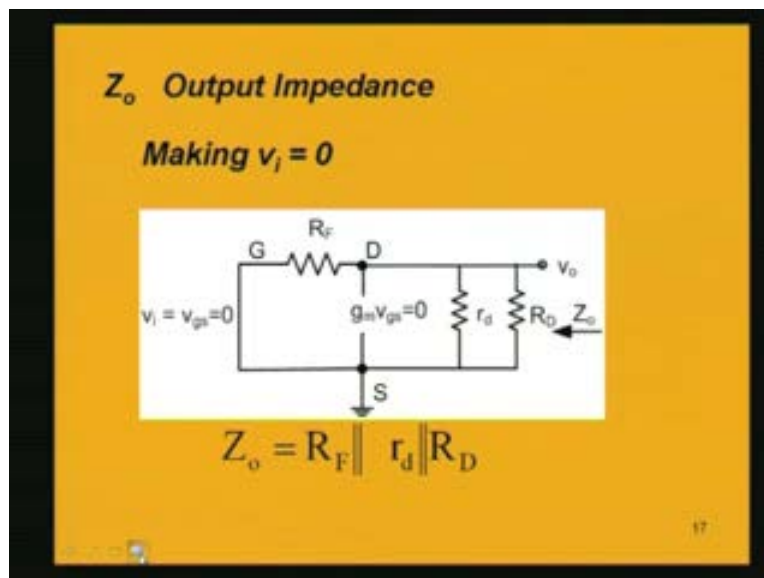
$$Z_i \cong \frac{R_F}{1 + g_m R_D}$$

if $r_d \geq 10R_D$

$r_d \parallel R_D \rightarrow R_D$

What will be the final expression? It is the simpler version of this whole original expression. It is capital R_F by 1 plus g_m into capital R capital D . We get the input impedance. Now let us find out what is the output impedance?

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The way to find out the output impedance is by making the input voltage zero and looking from the output terminals what will be the output impedance? That can be found out by making input voltage zero. When you make input voltage v_i zero what happens? If you redraw the circuit we will get a circuit like this where input voltage is simply shorted. It is zero means it is grounded. Immediately another thing happens when we have v_i is equal to zero. v_i is nothing but gate to source voltage. v_i is equal to zero means v_{gs} also

equal to zero. That is why the current source becomes zero because we see that the current source is dependent upon v_{gs} . It is a dependent current source. That is symbolized by this diamond. It is a dependent current source whose magnitude is dependent upon the voltage v_{gs} .

If v_{gs} is equal to zero, this part is also zero. So this part is like open circuited. Now it will be open circuit between the drain and source. We do not have the current source here. Rest of the circuit remains the same because we have this resistance R_F , r_d and R_D ; all are there. If we look from this side, output side what is output impedance Z_o ? It is simply the parallel combination of these three resistances. It is very clear from this circuit diagram that if we look from this output terminals there are three resistances in parallel. So the equivalent will be the three parallel resistances. So we have Z_o equal to R_F parallel small r_d parallel R_D . Again we can further approximate just following the earlier procedure. As R_F is quite large the parallel combination will ultimately have small r_d parallel R_D . That will be the output impedance as R_F is quite large. Again if the small r_d is equal to or greater than 10 times R_D , then we can write down this output impedance as simply R_D because the value of this small r_d parallel R_D will approach R_D when we have small r_d is very, very high as compared to R_D .

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$$Z_o \cong r_d \parallel R_D$$

if $R_F \gg r_d \parallel R_D$

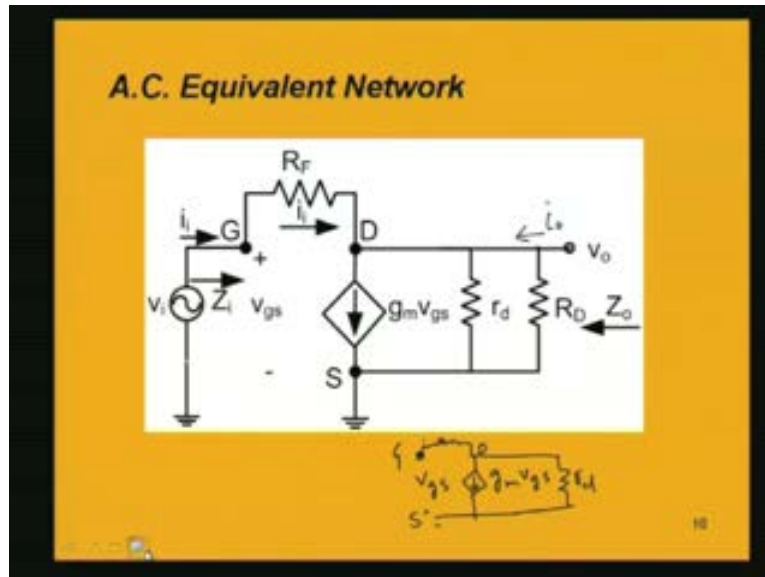
$$Z_o \cong R_D$$

if $r_d \geq 10R_D$

We have two parallel resistances. The equivalent will approach the smaller one and this is the thumb rule which says that we can use this approximation if this condition of small r_d being greater than equal to at least 10 times R_D is met. After this let us find out another important parameter which is basically the most important parameter as far as the amplifier is concerned which is voltage gain because we are using the amplifier for voltage gain only. We are trying to get an amplified output from a weak signal. In order to find out the voltage gain which is nothing but $A_v = v_o$ by v_i , to know what is the ratio

between v_o and v_i , let us again look into the circuit. In the circuit if you look into the drain terminal where we are going to use the Kirchoff's current law, as earlier we have used, i_i equal to $g_m v_{gs}$ plus this v_o divided by r_d parallel capital R_D .

(Refer Slide Time: 49:18)



We will use again sum of the incoming current is equal to sum of the outgoing current. That is what this expression is. Again v_{gs} is nothing but v_i . Replacing v_{gs} by v_i , we get this expression.

(Refer Slide Time: 49:35)

A_v Voltage Gain

Applying KCL at node D $A_v = \frac{V_o}{V_i}$

$$i_i = g_m v_{gs} + \frac{V_o}{r_d \parallel R_D}$$

$$= g_m v_i + \frac{V_o}{r_d \parallel R_D}$$

The current i_i is equal to v_i minus v_o by R_F . Here v_i minus v_o by R_F is equal to i_i . That is going to be used again like we proceeded in input impedance. This current and the expression which is earlier found will make them equal. That is this current i_i which is given by this expression (Refer Slide Time: 49:35) is written in another way; from the node voltages v_i minus v_o by R_F that is equal to this one.

(Refer Slide Time: 50:23)

Again, $i_i = \frac{v_i - v_o}{R_F}$

$$\frac{v_i - v_o}{R_F} = g_m v_i + \frac{V_o}{r_d \parallel R_D}$$

$$\frac{v_i}{R_F} - \frac{v_o}{R_F} = g_m v_i + \frac{V_o}{r_d \parallel R_D}$$

A little manipulation algebraically and we will further simplify the expression. If we write now v_i by R_F minus v_o by R_F is equal to $g_m v_i$ plus v_o by r_d parallel capital R_D . Taking v_o common, we have two terms having v_o . These two terms and another two terms are having v_i . These two terms are having v_o . We gather the terms having v_o and

the terms having v_i , v_o if we take common it will be 1 by R_F plus 1 by r_d parallel R_D and taking v_i common we get 1 by R_F minus g_m .

(Refer Slide Time: 51:26)

$$v_o \left[\frac{1}{r_d \parallel R_D} + \frac{1}{R_F} \right] = v_i \left[\frac{1}{R_F} - g_m \right]$$

$$A_v = \frac{v_o}{v_i} = \frac{\left[\frac{1}{R_F} - g_m \right]}{\left[\frac{1}{r_d \parallel R_D} + \frac{1}{R_F} \right]}$$

Our aim is to find the ratio between the v_o and v_i that is the voltage gain. The voltage gain is equal to v_o by v_i that is equal to 1 by R_F minus g_m divided by 1 by small r_d parallel R_D plus 1 by R_F . Look at the denominator term in the expression. What does this term mean? We see that this is nothing but the reciprocal of the parallel combination between capital R_D and capital R_F because if we take the reciprocal of small r_d parallel capital R_D parallel capital R_F , then we have this expression. r_d parallel R_D into this, if I do the algebraic simplification here then we will finally get reciprocal of this parallel. You can do this and verify and the numerator term is 1 by R_F minus g_m . This is our expression.

Now we can simplify. Of the two terms in the numerator one is the transconductance other is reciprocal of feedback resistance. We know that the feedback resistance is having a very high value, so its reciprocal will be a small value. Compared with this g_m , 1 by R_F is quite smaller. g_m is actually greater compared with 1 by R_F . Conveniently we can ignore now 1 by R_F in the numerator because minus g_m plus 1 by R_F is almost equal to minus g_m . We will do that.

(Refer Slide Time: 54:01)

$$A_v = \frac{V_o}{V_i} = \frac{\left[\frac{1}{R_F} - g_m \right]}{1 \over r_d \parallel R_D \parallel R_F}$$

Handwritten notes below the equation:

- $-g_m + \frac{1}{R_F}$
- $\approx -g_m$
- g_m
- $g_m \gg \frac{1}{R_F}$
- $\frac{1}{R_F}$

Here only minus g_m and in the denominator this term is there. Finally we get an expression that is minus g_m into this denominator will go up into small r_d parallel capital R_D parallel capital R_F . This is the exact expression for the voltage gain.

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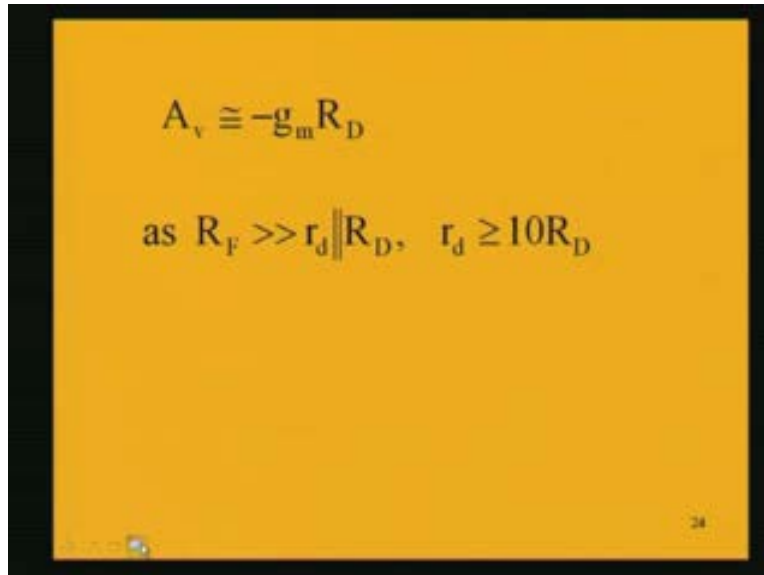
$$g_m \gg \frac{1}{R_F}$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{-g_m}{1 \over r_d \parallel R_D \parallel R_F} = -g_m (r_d \parallel R_D \parallel R_F)$$

For this feedback biasing scheme that is the drain feedback biasing scheme used for this MOSFET amplifier we get the voltage gain as minus g_m into small r_d parallel capital R_D parallel capital R_F . One important point to notice here is that there is a minus sign. It symbolizes the phase reversal between the input and the output. The output voltage will be 180 degree out of phase with the input voltage. As we have seen earlier in case of BJT amplifiers also when we were using common emitter amplifier we got that. Similarly here

in this common source amplifier there is a phase reversal of 180 degree between input and output voltage.

(Refer Slide Time: 55:27)


$$A_v \cong -g_m R_D$$
$$\text{as } R_F \gg r_d \parallel R_D, \quad r_d \geq 10R_D$$

A little more step can be done for approximating because we know that the feedback resistance is quite high as compared to r_d parallel capital R_D . This R_F is quite high value as compared to the parallel combination between these two resistances. We can write down here only r_d parallel R_D because here if we follow this we will ignore R_F as well. Further approximation can be done if small r_d is greater than equal to 10 times capital R_D , then we can also ignore small r_d .

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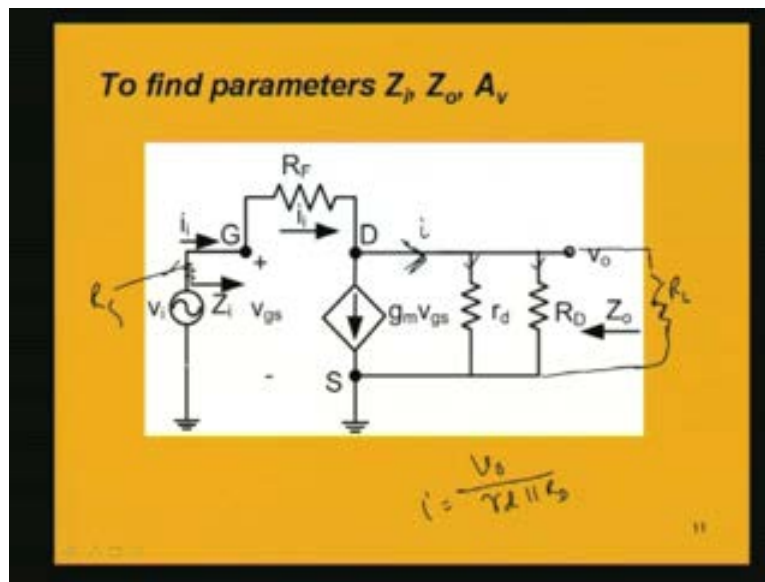
$$g_m \gg \frac{1}{R_F}$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{-g_m}{\frac{1}{r_d \parallel R_D \parallel R_F}} = -g_m (r_d \parallel R_D \parallel R_F)$$

$r_d \gg 10 R_D$
 $R_F \gg r_d \parallel R_D$

Finally what will remain is minus g_m capital R_D . Our voltage gain is dependent upon the transconductance and the drain resistance. The voltage gain can be increased if we adjust this drain resistance. But that is also a tricky matter because we have to basically see many things while designing an amplifier. In this analysis one thing to be noted is that we have not considered source resistance and load resistance yet. We were finding out the voltage gain from the open circuited voltage at the output. That is we are not using the load resistance at the output, we were simply taking open circuit voltage.

Similarly the resistance in the source was not considered. We know that the source generally has a small resistance in series with it and if we now consider the source resistance and the load resistance, in the equivalent circuit we will also have to consider these two resistances and put it into the circuit. That you can do simply if we redraw the AC equivalent circuit and include these resistances here and here. If we consider a load resistance here there will be R_L and if we consider a source resistance there will be a source resistance here. Correspondingly we will have to consider those in the relevant calculations.



That you can do easily and we have so far been able to find out the important parameters concerned with the common source MOSFET amplifier.

What we have done today is we have first of all found out the small signal model for a MOSFET device and then we used the MOSFET devices small signal model in an amplifier using the feedback biasing scheme and we proceeded to find out the important parameters which are related to amplifier which are the input impedance, output impedance and the voltage gain. We have found these by incorporating the small signal model into the amplifier network and then drawing the AC equivalent network for the whole amplifier circuit and then using the relevant electrical laws like Kirchoff's current law or voltage law in the AC equivalent circuit we found out the input impedance, output impedance and voltage gain and we discussed the e-MOSFET or enhancement type of MOSFET and in the next classes we will discuss about other biasing scheme for the device like voltage divider biasing scheme and we will see how these parameters can be obtained.